SCALABLE TWO TRANSISTOR MEMORY DEVICES AND METHODS OF FABRICATION THEREFOR

ABSTRACT OF THE DISCLOSURE

A memory device includes a semiconductor substrate, a first gate insulator on a first portion of a semiconductor substrate, a storage node on the first gate insulator, a tunnel junction barrier on the storage node and a data electrode on the layer tunnel junction barrier. The device further includes a second gate insulator layer on a sidewall of the tunnel junction barrier, a third gate insulator on a second portion of the substrate adjacent the tunnel junction barrier and a gate electrode on the second gate insulator and the third gate insulator. First and second impurity-doped regions are disposed in the substrate and are coupled by a channel through the first and second portions of the substrate. Fabrication of such a device is also describes.